Hardware Manual
for
PCIE1L-1553

Part Number: 15191-00000-A9
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Alta Data Technologies LLC
4901 Rockaway Blvd, Building A
Rio Rancho, NM 87124 USA
(tel) 505-994-3111 • www.altadt.com

CUSTOMER NOTES:

Revision Control History

Rev A9 Release Date: 16 January 2023

Note to the Reader and End-User:

Contact:

We welcome comments and suggestions. Please contact us at 888-429-1553 (toll free in US) or 505-994-3111 or visit our web site for support submit forms at www.altadt.com.

PCIE1L-1553
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PCIE1L-1553 Hardware Manual

Introduction

This manual provides detailed hardware information on the PCIE1L-1553 interface card.

In addition to this information, the reader may also want to reference the following documents provided on the CD and our Web Site

- **AltaCore™** Specifications and User Manual: Detailed description of the 1553 protocol engine of the card. Most people do not need this detail and will mainly reference the **AltaAPI** manual for their application development.
- **AltaAPI™** User's Manual: Detailed description of the application program interface (API) and device drivers of this software package.
- **AltaView™** User's Manual: AltaView is the latest 1553 analyzer on the market and this manual details the usage of the product.
- **AltaRTVal™** User's Manual: This manual details the usage of AltaRTVal, which is an automated program to run AS4111/4112 RT Validation and Production Test Plans.
- 1553 Tutorial and Reference, and 1553B Standard. These documents provide a detailed review of the 1553 standard, which is required for proper usage of this product. **SEE THIS DOCUMENT FOR WIRE & CABLING INFORMATION OF 1553 BUSSES – THIS IS REQUIRED FOR PROPER BUS OPERATIONS.**

ESD and General Handling of Computer Interface Cards

The Alta warranty requires that the product be handled with proper ESD controls. The JEDEC standard on ESD handling, JESD625-A, is available for free download at www.jedec.org. Please follow the standard's guideline for proper ESD handling methods. At a minimum the following guidelines should be followed:

- Avoid carpets in cool, dry areas.
- Leave the card in its anti-static packaging until ready to be installed.
- Dissipate static electricity before handling the card by touching a grounded metal object, such as the metal chassis of the system (the system should be plugged-in, but turned-off).
- Use antistatic devices, such as wrist straps and floor mats.
- Always hold the card by its edges. Avoid touching the components or connectors.
- Be sure to align card edge or assembly cable connector pins before installation. Misaligned connectors can cause damage to the card or system, especially at power-on.
- Take care when connecting or disconnecting cables. When disconnecting a cable, always pull on the cable connector, not on the cable itself.

PCIE1L-1553 Description

The Alta PCIE1L-1553 is a Low Profile PCI Express 1 Lane card. This interface card is a multi-channel (1-2) 1553 bus interface supported by the latest software technologies and is based on the industry's most advanced 32-bit 1553 FPGA protocol engine, ***AltaCore***™, and by a feature-rich application programming interface, ***AltaAPI***™, which is a multi-layer ANSI C and Windows.NET (MSVS C++, C#, VB .NET) architecture. This hardware and software package provides increased system performance and reduces integration time.

The cable assembly pin-outs are provided in Appendix A of this document.

Card Level Specifications

- Low Profile PCI Express 1 Lane Card
- PCI Express 1.1 Compliant with MSI Support
- Up to Two MIL-STD-1553 Channels
    - Transformer Coupled Stub Interface Standard
    - Direct Coupled Stub Interface available upon request
- 2 Mbytes of SRAM memory
- IRIG-B Receiver (DC or AM)
- Signal Capture capability on Channel One
- 8 Single-Ended Bi-Directional Avionics Discretes
- Two RS-485 Discretes
- One LVTTL Input and Output Trigger per Channel
- External Input and Output Clocks (LVTTL or RS-485 Selectable)
- 1760 Ext RT Addressing
- Two Temperature Sensors
- Required Power: 1.5A(Max)@3.3V
- 5.0 Watts Max (Two Channel)
- Operating Temperature range: 0-70C Standard
    - -40 to +85C Extended Temp Parts with –E Option (as applicable).
- Relative humidity: 5 to 95% (non-condensing).
- RoHS Compliant

MTBF

Please contact your Local Sales Representative or Alta Technical Support for additional information regarding any concerns or questions that may arise regarding MTBF for the PCIE1L-1553.

Environment: Ground Benign, 25C

Table 1. MTBF

Channel Count	MTBF
1	792,762 hrs
2	768,949 hrs

PCIE1L-1553 Photographs

The following pictures show the front side and front panel of the PCIE1L-1553 card.

Figure 1. PCIE1L-1553 Front Side

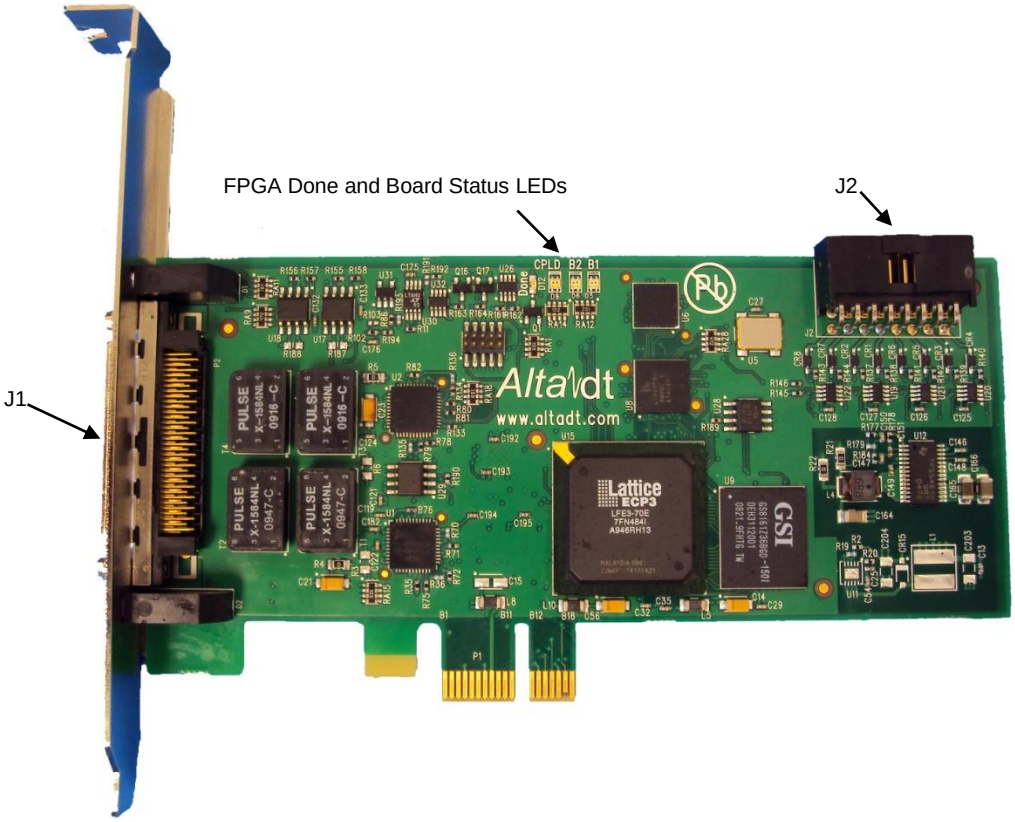
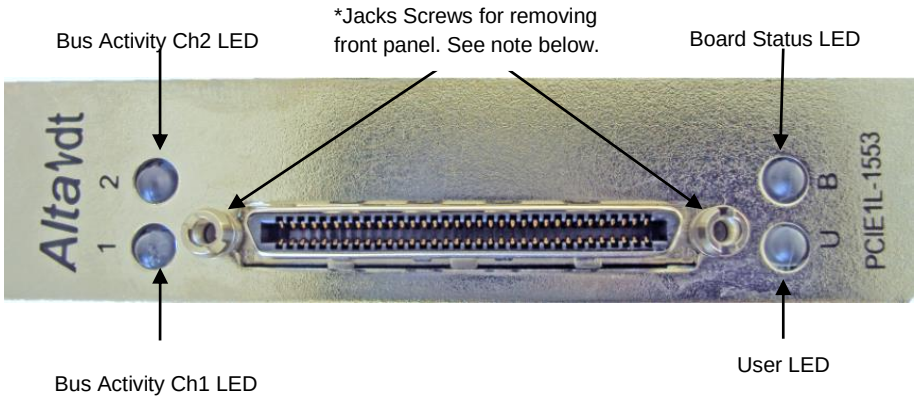


Figure 2. PCIE1L-1553 Front Panel



*Note: PCIE1L-1553 boards are shipped with both standard height and low profile front panels. To change panels, remove the two jack screws noted in the figure above, replace the panel, and re-install the jack screws. Do not over tighten the jack screws as this could cause permanent damage to the connector.

LED Descriptions

Table 2. LED Descriptions

LED	Name	Description
Front	Channel One 1553 Bus Activity	Green=No Errors, Red=Errors Detected
Front	Channel Two 1553 Bus Activity	Green=No Errors, Red=Errors Detected
Front	Board Status	Green=No Error, Red=BIT Error Detected on at least one channel.
Front	User LED	Set on or off by the User – Red/Green/Amber
D5	Channel One BIT Status	Green=No Errors, Red=Errors Detected
D6	Channel Two BIT Status	Green=No Errors, Red=Errors Detected
D9	Board Status	Green=No Error, Red=FPGA Load Error Amber= Power Supply Failure
D12	FPGA Loaded	Green=FPGA Loaded, Off=FPGA Not Loaded

PCI/PCI Express Device Information

PCI Device ID: 0x0020
PCI Vendor ID: 0xAD00

The table below explains the memory regions that should be mapped by the host.

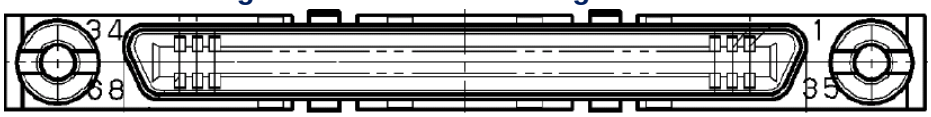
Table 3. Host Mapping

Base Address Reg	Type	Size (Bytes)	Description
BAR 0	Memory	512	Local Configuration Registers (Mapped)
BAR 1	N/A		Not Used
BAR 2	Memory	4 Meg	User Memory Space (Mapped)
BAR 3-5	N/A		Not Used

Connectors

J1 (Front Panel)

Figure 3. Connector Facing the Card

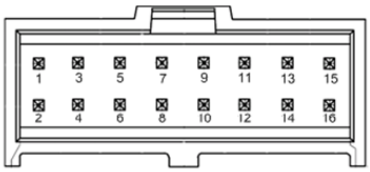


The following table provides pin-outs for the J1 Front Panel connector.

Table 4. J1- 68-pin Connector

J1 Pin#	Signal	J1 Pin#	Signal
1	1553 CH1A +	35	N/C
2	1553 CH1A -	36	N/C
3	1553 Shield	37	N/C
4	1553 CH1B +	38	N/C
5	1553 CH1B -	39	N/C
6	1553 Shield	40	N/C
7	1553 CH2A +	41	N/C
8	1553 CH2A -	42	N/C
9	1553 Shield	43	N/C
10	1553 CH2B +	44	N/C
11	1553 CH2B -	45	N/C
12	1553 Shield	46	N/C
13	TRIG_IN1	47	N/C
14	TRIG_OUT1	48	N/C
15	TRIG_IN2	49	N/C
16	TRIG_OUT2	50	N/C
17	GND	51	N/C
18	~AutoTest	52	N/C
19	RS-485_2+	53	N/C
20	RS-485_2-	54	N/C
21	N/C	55	N/C
22	N/C	56	N/C
23	N/C	57	N/C
24	RS-485_1+	58	N/C
25	RS-485_1-	59	N/C
26	EXT TTL IO	60	N/C
27	GND	61	N/C
28	IRIG In	62	N/C
29	IRIG GND	63	N/C
30	JTAG PWR	64	N/C
31	JTAG CLK	65	N/C
32	JTAG TMS	66	N/C
33	JTAG TDI	67	N/C
34	JTAG TDO	68	N/C

J2 (Aux)



The following table provides pin-outs for the J2 Auxiliary Connector.

Table 5. J2- 16-pin Connector

HDR Pin	Signal	HDR Pin	Signal
1	SDISC1 / RTADDR1_0	2	GND
3	SDISC2 / RTADDR1_1	4	GND
5	SDISC3 / RTADDR1_2	6	GND
7	SDISC4 / RTADDR1_3	8	GND
9	SDISC5 / RTADDR1_4	10	GND
11	SDISC6 / RTADDR1_P	12	GND
13	SDISC7	14	GND
15	SDISC8	16	~RTADDR_EN

Signal Capture Discussion

The PCIE1L-1553 HW provides Signal Capture capability on Channel One. The Signal Capture feature uses an analog-to-digital converter (ADC) to capture the electrical signal on the selected 1553 stub (A or B). The Signal Capture feature will capture 2048 samples at a rate of 20MHz, or 50 nanoseconds per sample. Therefore the sample buffer contains 102.4 microseconds of data. Each sample is an 8-bit (256 step) value representing the differential voltage on the 1553 stub.

To convert the raw ADC data to a stub voltage representation, use the following formula:

Stub Voltage = (ADC data – 128) * 1.79 (xformer ratio) * 32 (voltage divider) * 2mv (step voltage)

Reducing the above gives:
Stub Voltage = (ADC data – 128) * 0.11456

WARNING: The Signal Capture data should be accurate to within 500mV. The Signal Capture Feature does NOT replace a calibrated oscilloscope for voltage or timing measurements on the 1553 stub. The Signal Capture Feature provides simple voltage and timing data. If more precise information is needed regarding the electrical signal on the 1553 bus, a real oscilloscope should be used.

The following steps should be performed to acquire Signal Capture data from the PE. See the *AltaCore-1553* User's Manual for more information on the Signal Capture CSR and Data Registers.

1. Set the Trigger on Any Activity bit in the Signal Capture CSR
2. Wait for Data Ready bit to get set in the Signal Capture CSR
3. Read data from the Signal Capture Data Register. Note: The Data Register contains four samples.
4. Keep reading data until the FIFO Not Empty bit is set to zero by the PE.

Host Memory Map

The figure below shows the basic memory map configuration for a 2 channel PCIE1L-1553 interface with one megabyte of RAM per channel Special configurations may vary.

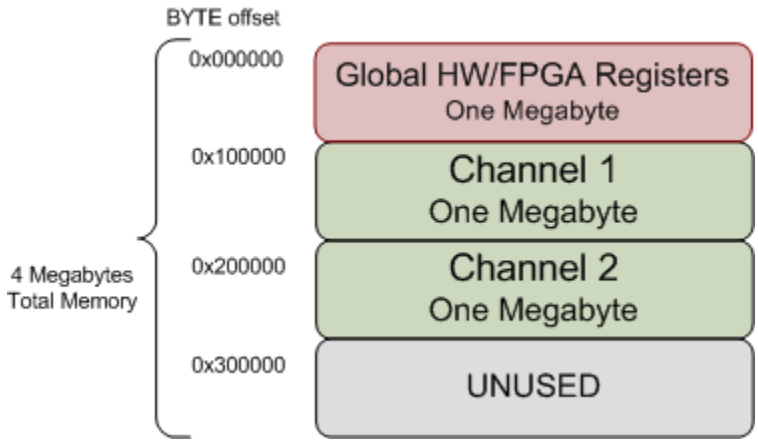


Figure 4. Basic Memory Map

Global Registers

The first Megabyte of the PCIE1L-1553 memory map contains backplane and global card level settings and status values that affect processing for all channels. Details on Global Registers may be found in the AltaCore-1553 Spec User's manual.

Revision Information

Date	Rev	Description
2/01/10	A	Initial Release
4/20/10	A1	Added Bookmark to PDF
2/14/11	A2	Removed Global Figure's
3/9/12	A3	Added Bookmark to PDF
02/24/15	A4	Updated NAICS #
10/12/15	A5	Added Cable assembly information
01/31/17	A6	Updated cable information to include whether or not cables contain PVC
11/08/21	A7	Updated picture in Appendix A to include cable with AUX
05/05/22	A8	Updated MTBF section and corrected numbers in Table1.
01/16/23	A9	Updated Card Level Specifications and contact info Updated Appendix A. to state that cables are optional Removed revision and date from board description

Appendix A: Cable Assembly Information

Alta Cable Assembly Part Numbers (Reorder Numbers)

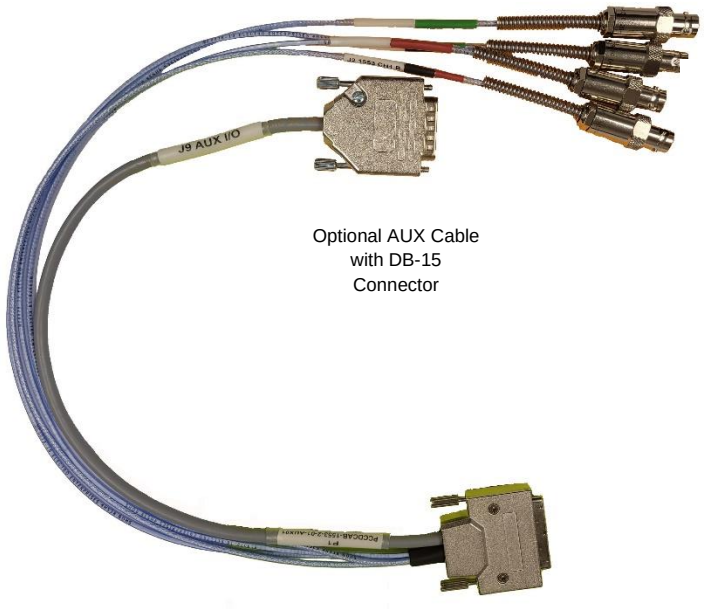
(The following assemblies are **optional** item shipments..
They DO NOT have the AUX DB-15 Connector)
PCCDCAB-1553-1-01 (one channel*)
PCCDCAB-1553-2-01 (two channel*)
PCCDCAB-1553-1-02 (one channel with 180 Degree Backshell Orientation*)
PCCDCAB-1553-2-02 (two channel with 180 Degree Backshell Orientation*)

(The following assemblies are **optional** item shipments..
They DO have the AUX DB-15 Connector)
PCCDCAB-1553-1-AUX01 (one channel with DB-15**)
PCCDCAB-1553-2-AUX01 (two channel with DB-15**)
PCCDCAB-1553-1-AUX02 (one channel with DB-15 and 180 Degree Backshell Orientation**)
PCCDCAB-1553-2-AUX02 (two channel with DB-15 and 180 Degree Backshell Orientation**)

* Does not contain PVC
** Contains PVC

Honda Connector Information:
Backshell: Components Express #191-000002-010 (or equivalent)
Honda Connector: #HDRA-68BA (or equivalent)
PCB (Con-01): Alta# 62007-00000

Figure 1: PCCDCAB-1553-2-AUX01



1553 3-Slot Female Connectors

Optional AUX Cable with DB-15 Connector

Cables are EU and China RoHS Compliant.
RoHS 2002/95/EC

Cable Assembly Markings & Information:

- **1553 Connectors are 3-Lug (BJ-77 Type) Female Connectors**
- 1” from Connector Base Label: Cable Part Number
- 1553 Cable Labeling – Shrink Wrap Color Code
    - 1” from base of connector add Shrink Wrap Color Code
        - CH1 A – Shrink Tube Color Code: Red
        - CH1 B –Shrink Tube Color Code: Red-Black Stripe
        - CH2 A – Shrink Tube Color Code: Green
        - CH2 B –Shrink Tube Color Code: Green-Black Stripe
    - 2” from base of connector label text:
        - **J1 1553 CH1 A**
        - **J2 1553 CH1 B**
        - **J3 1553 CH2 A**
        - **J4 1553 CH2 B**
- DB15 AUX Connector Labeling – Optional Connector
    - 1” from base of connector add label
        - **J9 AUX I/O**
- 24” length on 1553 cables (tip to tip – including connectors).
- 18” length on DB15 AUX Cable (tip to tip – including connectors).
- 1553 thin Cable with 1553 Connector
- Assembly Standard: IPC-610 Class 3/RoHS
- Assemble with Lead free components and Lead free solder.

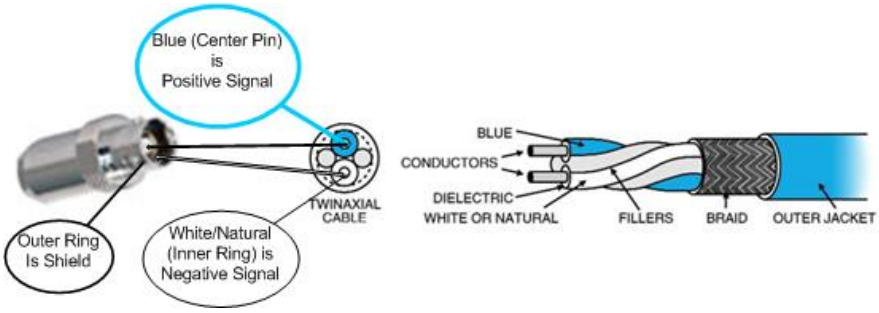


Table 6: Connector to DB15 Cross Reference
(Optional Connector)

DB-15	Honda CON	Signal
1	13	TRIG IN1
2	14	TRIG OUT1
3	15	TRIG IN2
4	16	TRIG OUT2
5	17	GND
6	18	~AUTO_TEST
7	19	DDISC2+
8	20	DDISC2-
9	24	DDISC1+
10	25	DDISC1-
11	26	EXT_TTL_IO
12	27	GND
13	28	IRIG IN
14	29	GND
15	-	NC